**Details about 3 assembly instruction of MIPS FPGA :**

I found the following informations in the MIPS32 Instruction Set Architecture

**BEQ** :Branch on equal

**Format** : BEQ rs, rt, offset

**Purpose** : To compare GPRs then do a PC-relative conditional branch

**Description** : if rs = rt then branch An 18-bit signed offset (the 16-bit offset field shifted left 2 bits) is added to the address of the instruction following the branch (not the branch itself), in the branch delay slot, to form a PC-relative effective target address. If the contents of GPR rs and GPR rt are equal, branch to the effective target address after the instruction in the delay slot is executed.

**MFC0 :** Move From Coprecessor 0

**Format** : MFC0 rt, rd

**Purpose** : To move the contents of a coprocessor 0 register to a general register.

**Description** : rt ← CPR[0,rd,sel] The contents of the coprocessor 0 register specified by the combination of rd and sel are loaded into general register rt. Note that not all coprocessor 0 registers support the sel field. In those instances, the sel field must be zero.

**EXT** : Extract Bit Field

**Format** : ext rt, rs, pos, size

**Purpose**: To extract a bit field from GPR rs and store it right-justified into GPR rt.

**Description** : rt ← ExtractField(rs, msbd, lsb) The bit field starting at bit pos and extending for size bits is extracted from GPR rs and stored zero-extended and right-justified in GPR rt. The assembly language arguments pos and size are converted by the assembler to the instruction fields msbd (the most significant bit of the destination field in GPR rt), in instruction bits 15..11, and lsb (least significant bit of the source field in GPR rs), in instruction bits 10..6, as follows: msbd ← size-1 lsb ← pos The values of pos and size must satisfy all of the following relations: 0 ≤ pos < 32 0 < size ≤ 32 0 < pos+size ≤ 32